Fig. 9 is a top plan view of a third embodiment of an active integrated circuit structure made up of components formed on two different layers with proper alignment.

Fig. 10 is a top plan view of the active integrated circuit structure of Fig. 9 with the different layer components misaligned.

Fig. 11 is a top plan view of a measurement structure corresponding substantially to the active integrated circuit structure of Fig. 9, formed in the wafer kerf area and having the different layer components displaced.

Fig. 12 is a top plan view of a measurement structure corresponding substantially to the misaligned active integrated circuit structure of Fig. 10, formed in the wafer kerf area and having the different layer components displaced.

Fig. 13 is a top plan view of a silicon wafer showing the second embodiment active circuit structures inside the individual product cells and the corresponding overlay measurement structures in the kerf areas separating the product cells.

Fig. 14 is a close up showing one product cell containing the active circuit structures and one corresponding kerf measurement structure.

Description of the Preferred Embodiment(s)

In describing the preferred embodiment of the present invention, reference will be made herein to Figs. 1-14 of the drawings in which like numerals refer to like features of the invention. Features of the invention are not necessarily shown to scale in the drawings.

In order to easily correlate the conventional overlay measurement to device overlay, the present invention provides a system and method of representing a measurable device structure in the kerf area, between the printed functional circuit areas, to aid in direct device overlay measurement. The present invention is based on a method that allows the overlay to be determined on circuit size and shaped device patterns without the difficulty related to pattern-on-pattern placement. To accomplish

this, in the preferred embodiment the device design itself is printed in the kerf, with two patterns being printed not on top of each other, but physically separated in at least one dimension. This permits the use of high resolution microscopy to measure edge or centerline overlay error without the confluence of edges. The preferred kerf measurement structures use the actual device design, displaced relative to each other allowing easily discernible edges of each structure. They are still located symmetrically about each other such that conventional edge or centerline overlay measurements may still be made.

A typical pattern made in a dynamic random access memory (DRAM) chip is made up of a plurality of active circuit areas separated by the kerf areas, also known as streets. A typical memory device cell has many active areas that need to be aligned between different lithographically produced levels. In practice, however, the active circuit areas on one level may misalign with respect to active circuit areas on another level and cause short and/or open circuits. To obtain an error measurement of how far the different levels are displaced, the present invention takes the same structure or design features as in the active circuit area, or structures that are substantially corresponding to them, and actually places them in the kerf region and separates them in one dimension. The separation need not be a known amount, so long as the two edges on the two different layers can be clearly discerned and one can determine a centerline estimate of overlay misalignment.

By a substantially corresponding structure or design feature is meant that the structure or design feature is substantially replicated with respect to the features in issue, for example edges, and under the same design rule. Preferably, the kerf measurement feature is reproduced as closely as practical, and more preferably the kerf measurement feature replicates the size and pitch of the corresponding active feature in the circuit pattern, as well as its shape and its proximity to other structures, as closely as possible. Thus, the kerf measurement feature corresponds substantially to the corresponding active circuit feature.

In accordance with the present invention, instead of overlaying the measurement features from different layers on top of each other in the kerf area, they are displaced or separated by some amount, in a direction normal to the direction of overly error measurement, such that one can easily more obtain a measurement of what the overly misalignment is between them. The location in the kerf measurement structure is not normally important in practicing the present invention, and can be at random in various places, or it can be at one set reference location. A kerf measurement structure is separated from its corresponding similar active structure in the circuit area on each level, and the degree of separation in one of the x- or y-dimension is by the same distance. Further, each layer's kerf measurement structure should be displaced or separated in the dimension 90° or perpendicular to the direction of overlay error measurement so that the edges can be clearly identified for each layer, and the measurement structures of the two layers are not superimposed upon each other. The two kerf measurement features on the different layers need not be completely separated, but should be displaced by some amount so that features on each can be distinguished. For example, where the overlay error measurement is to be made in the y-dimension, the amount of the x-dimension separation is immaterial, as long as the kerf measurement features of the two layers which are difficult to discern in the active structure are physically displaced or separated in the kerf by a sufficient distance so that the separate layer features are easier to discern. However, in each layer the distance of separation or offset between the active feature in the circuit pattern and the measurement feature in the kerf area, in the direction of the offset error measurement (e.g., the y-direction), has to be identical. This distance of separation in the direction of overlay error measurement may range from zero to any maximum that enables the active circuit structures and the corresponding kerf measurement structures to fit on the wafer.

A first example of the present invention is depicted in Figs. 1-4 which shows active circuit structures 20 and 22, in an integrated circuit product cell on a semiconductor wafer, of the type that may be created in two separate